REMARKS

Claims 1-20 are pending in the current application. Claims 1, 7, 10 and 20 are independent claims.

35 U.S.C. § 112, First Paragraph

Claims 1-9 and 12-19 stand rejected under 35 U.S.C. § 112, first paragraph failing to comply with the written description requirement. Applicant respectfully traverses this rejection.

With regard to claims 1, 7 and 15, the Examiner alleges that "a selecting circuit for determining an operational state of the processor" as recited in independent claim 1 and similarly recited in claims 7 and 15 is unclear (see page 2 of the Office Action). The Examiner further alleges that the "selecting circuit" as cited in claims 3, 4, 9 and 12-14 is likewise unclear. The Examiner's confusion appears to be directed to whether the above claim limitations read on the specification in paragraph [0028] or paragraph [0031]. Applicant respectfully submits that the claim language in question may read on both paragraph [0028] and paragraph [0031].

Paragraph [0028] describes a broader functionality of the selecting circuit 220. Paragraph [0028] deals with a checking or monitoring of either an operational mode or an operational frequency, and further discloses that a selection signal SEL may be output to the MUX 250 in response to either monitoring. Paragraph [0031], on the other hand, describes a monitoring of the state or operation mode only, and not the operating frequency. Further, paragraph [0031] goes into more detail with respect to the operation mode monitoring as compared to paragraph [0028]. Accordingly, Applicant submits that it would be understood upon a review of the specification that the claim language may read on each of paragraphs [0028] and [0031].

35 U.S.C. § 112, Second Paragraph

Claims 1-9 stand rejected under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully traverses this rejection.

With regard to claim 1, the Examiner alleges that "the evaluation" lacks antecedent basis. The claim language "the evaluation" has been replaced by "the determination" by this amendment. Applicant respectfully submits that "the determination" has sufficient antecedent basis.

With regard to claim 3, the Examiner alleges that "the operating frequency" and "the compared result" lacks antecedent basis. With regard to "the operating frequency", Applicant respectfully submits that independent claim 1, upon which claim 3 is dependent, has been amended so as to include sufficient antecedent basis for "the operating frequency". With regard to "the compared result", Applicant respectfully submits that claim 3 now includes the language "the selecting circuit compares ... to obtain a compared result", and thereby "the compared result" now has sufficient antecedent basis.

With regard to claim 7, the Examiner alleges that "the evaluation" lacks sufficient antecedent basis. Applicant respectfully disagrees. Applicant respectfully submits that "the evaluation" may read on the "evaluating an operation mode or operation frequency of the processor". While the antecedent basis is not explicit, Applicant respectfully submits that it is clear for a reading of the claim as to what "the evaluation" refers to.

With regard to claim 9, the Examiner alleges that "the operating frequency" lacks sufficient antecedent basis. Applicant respectfully disagrees. Claim 9 is dependent upon claim 7. Claim 7 recites "evaluating an operation mode or operating frequency of the processor" (Emphasis added). Accordingly, Applicant respectfully submits that "the

operating frequency of the processor" as recited in claim 9 includes sufficient antecedent basis.

In view of the above remarks and compliant amendments, Applicant respectfully requests that the Examiner withdraw this rejection.

35 U.S.C. § 103(a) Kim in View of Dai and Further in View of Applicant Admitted Prior Art (AAPA)

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of Dai and further in view of AAPA. Applicant respectfully traverses this art grounds of rejection.

Kim is directed to a circuit and method of generating clock signals for a low power consumption CDMA modem chip design. In particular, Kim discloses a second clock generator 120 outputting a lower frequency clock signal CLOCK2 to a multiplexer 160 (e.g., see Figure 2 of Kim). The multiplexer 160 also receives a clock signal CLOCK1 at a higher frequency than the clock signal clock 2. The multiplexer 160 receives a clock selection signal from a clock selection unit 140. The selection signal received from the clock selection unit 140 is based on instructions received from a first clock controller 130. Claim 1 recites "a low speed and low power control circuit for controlling ... in response to the selection signal". The Examiner appears to read the claimed "low speed and low power control circuit" on the second clock generator 120 illustrated in Figure 2 of Kim. However, the second clock generator 120 of Kim does not receive any selection signal from the first clock controller 130 and/or the clock selection unit 140.

Applicant further agrees with the Examiner in that Kim:

> does not teach that the selecting circuit determines the operational state of the processor and outputs the selection signal based on the evaluation of the operational state of the processor. Additionally, Kim does not teach that the processor has a processor core and at least one peripheral device

(see page 4 of the Office Action).

The Examiner seeks to combine Dai and the AAPA with Kim in order to overcome the above-described deficiencies of Kim. The Examiner alleges that Dai discloses "selecting circuit [which] compares the operating frequency of the processor with a predetermined threshold frequency and outputs the selection signal based on the result" (page 5 of the Office Action) substantially in the Abstract lines 1-5 and paragraph [0013], lines 5-10 of Dai. Applicant respectfully disagrees.

Dai is directed to a method and apparatus to enhance processor power management. In particular, Dai discloses two operational states: a high performance state and a low power state. Dai associates that each of the two states are associated with predetermined core clock frequencies and supply voltage levels (see Abstract of Dai). However, the operating frequency of the processor of Dai is not compared with any threshold to determine whether or not to output a selection signal. The only determining factor with regard to which state the Dai processor is operating in accordance with appears to be whether the system is powered with an external power source or an internal battery (see paragraph [0013] of Dai). A review of Dai reveals that Dai does not disclose or suggest comparing an operating frequency of a processor with a threshold frequency to determine whether or not to output a selection signal for controlling an operation of the processor. Accordingly, the Examiner appears to be incorrect in asserting that "[d]epending on the processor frequency, the system may be selected to perform in high performance mode or low power mode" (see page 5 of the Office Action). Rather, the processor frequency appears to have nothing to do with the operating mode selection.

The Examiner then further seeks to combine the AAPA with Kim and Dai to overcome the deficiencies of Kim and Dai. However, a cursory review of the AAPA reveals

that the AAPA is similarly deficient in disclosing or suggesting the above-described deficiencies of the combination of Kim and Dai.

In view of the above remarks, Applicant respectfully submits that the combination of Kim, Dai and the AAPA cannot disclose or suggest "a selecting circuit for determining an operational state of the processor and for outputting a selection signal based on the determination" and "controlling high speed operations" and/or "low speed and low power operations" "in response to the selection signal" as recited in independent claim 1 and similarly recited in independent claim 7.

As such, claims 2-6 and 8-9, dependent upon independent claims 1 and 7, respectively, are likewise allowable over the combination of Kim, Dai and the AAPA for at least the reasons given above with respect to independent claims 1 and 7.

With respect to independent claims 10 and 20, the Examiner appears to reject each of claims 10 and 20 solely based on Kim and omits any reference to either Dai and/or the AAPA. Accordingly, Applicant will address the response to the rejections of claims 10 and 20 as if claims 10 and 20 were rejected based on Kim under 35 U.S.C. § 102.

Claim 10 is directed to a processor including "a circuit for selecting a control circuit from a plurality of control circuits, the control circuit for controlling one of at least a first device and a second device". The Examiner alleges that the circuit of claim 10 reads upon the clock selection unit 140 of Figure 2. Applicant respectfully disagrees.

With regard to the clock selection unit 140, Kim recites the following:

> The clock selection unit 140 outputs a selection signal for outputting one of the first and second clock signals CLOCK 1 and CLOCK 2 as a processor clock signal P_CLOCK, in response to a control signal that is outputted from the instruction decoder 150. Specifically, if [~~the~~] an instruction decoded in the instruction decoder 150 is a power-down instruction, the clock selection unit 140 outputs a selection signal 3 for selecting the second clock signal CLOCK2 in response to a control signal 1 that is inputted from the instruction decoder 150. Then, the clock selection unit 140 outputs a clock change end signal 4 to

> the first clock controller 130. If the decoded instruction is a power-up signal, the clock selection unit 140 outputs a selection signal E for selecting the first clock signal CLOCK1 in response to a control signal A outputted from the instruction decoder 150 and a first clock power-up end signal D inputted from the first clock controller 130.
>
> (Kim, paragraph [0017])

From the above-given description of the clock selection unit 140, it is unclear how the clock selection unit 140 is capable of "selecting a control circuit from a plurality of control circuits". Rather, the clock selection unit 140 appears to output a single selection signal which is used for selecting between clock signals at different frequencies. Namely, the selection signal output by the clock selection unit 140 is received by the multiplexer 160 to select between clock signals CLOCK1 and CLOCK2. Accordingly, the clock selection unit 140 selects between clock signals, and not control circuits. A clock generator is not necessarily a "control circuit". Accordingly, Applicant respectfully submits that Kim cannot disclose or suggest "selecting a control circuit from a plurality of control circuits, the control circuit for controlling one of at least a first device and a second device" as recited in independent claim 10 and similarly recited in independent claim 20.

As such, claims 11-19, depend upon independent claim 10, are likewise allowable over the combination of Kim, Dai and the AAPA for at least the reasons given above with respect to independent claim 10.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-20 in connection with the present application is earnestly solicited.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant(s) hereby petition(s) for a one (1) month extension of time for filing a reply to the outstanding Office Action and submit the required $120.00 extension fee herewith.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____
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